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| L3 | 710/113,244,240,116,41,243;711/147,154;709/221;340/825.5;370/431;714/13;327/19.ccls. | 613 |
| | *DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | |
| L2 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | |
| | *DB=PGPB,USPT,USOC; PLUR=YES; OP=OR* | |
| L1 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | |

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| (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | 6 |

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**Search:** L1

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| L1 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | 6 | L1 |

END OF SEARCH HISTORY

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# Refine Search

**Search Results -**

| Terms | Documents |
|---|---|
| (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | 1 |

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**Search:** L2

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## Search History

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| *DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L2 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | 1 | L2 |
| *DB=PGPB,USPT,USOC; PLUR=YES; OP=OR* | | | |
| L1 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | 6 | L1 |

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**Search Results -**

| Terms | Documents |
|---|---|
| L3 and L4 | 3 |

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**Search:** L5

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| L5 | l3 and L4 | 3 |
| L4 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4 or ticket) | 1( |
| L3 | 710/113,244,240,116,41,243;711/147,154;709/221;340/825.5;370/431;714/13;327/19.ccls. | 613 |
| | *DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | |
| L2 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | 1 |
| | *DB=PGPB,USPT,USOC; PLUR=YES; OP=OR* | |
| L1 | (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | ( |

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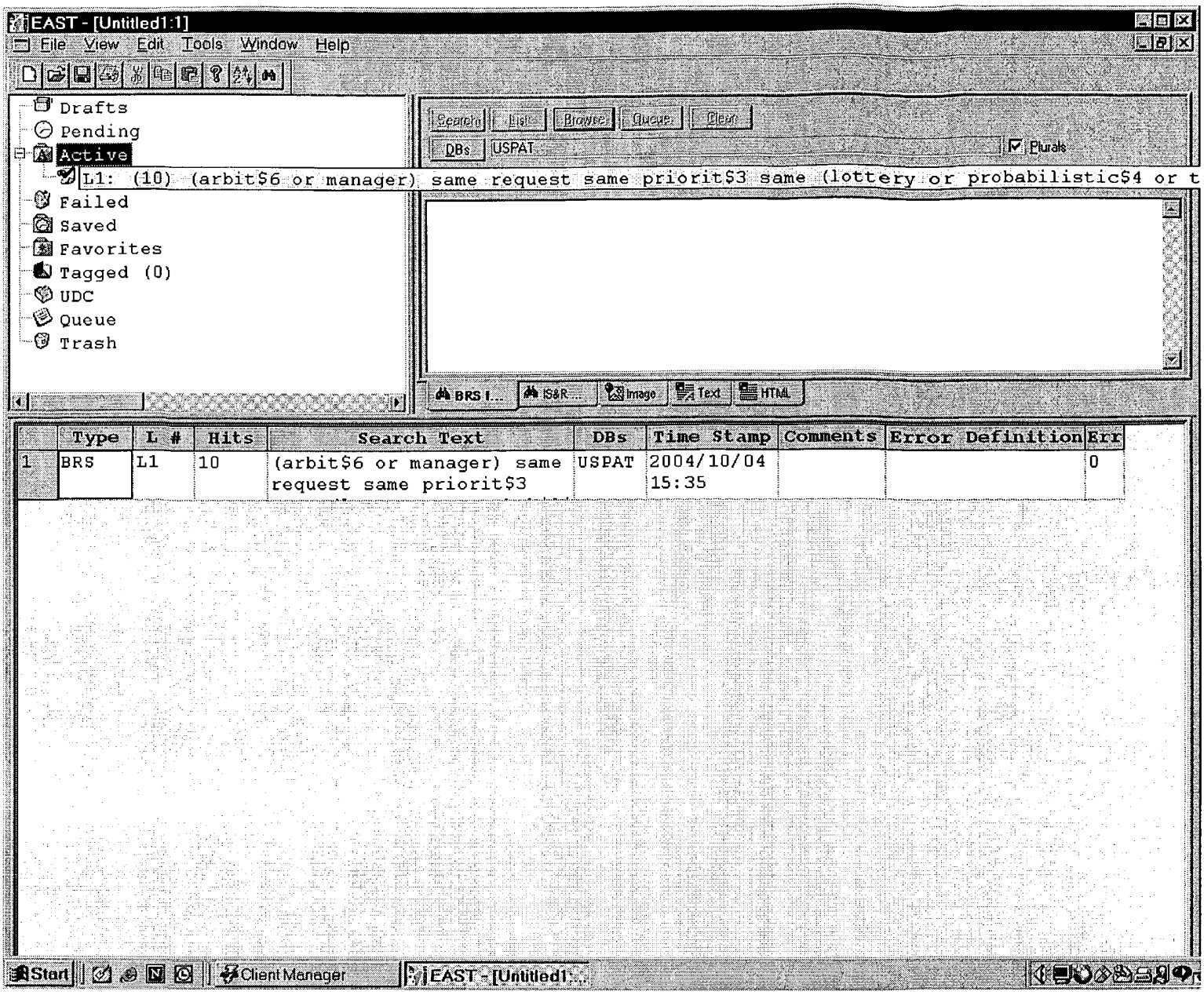
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1 | BRS | L1 | 10 | (arbit$6 or manager) same request same priorit$3 | USPAT | 2004/10/04 15:35 | | | 0
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Client Manager
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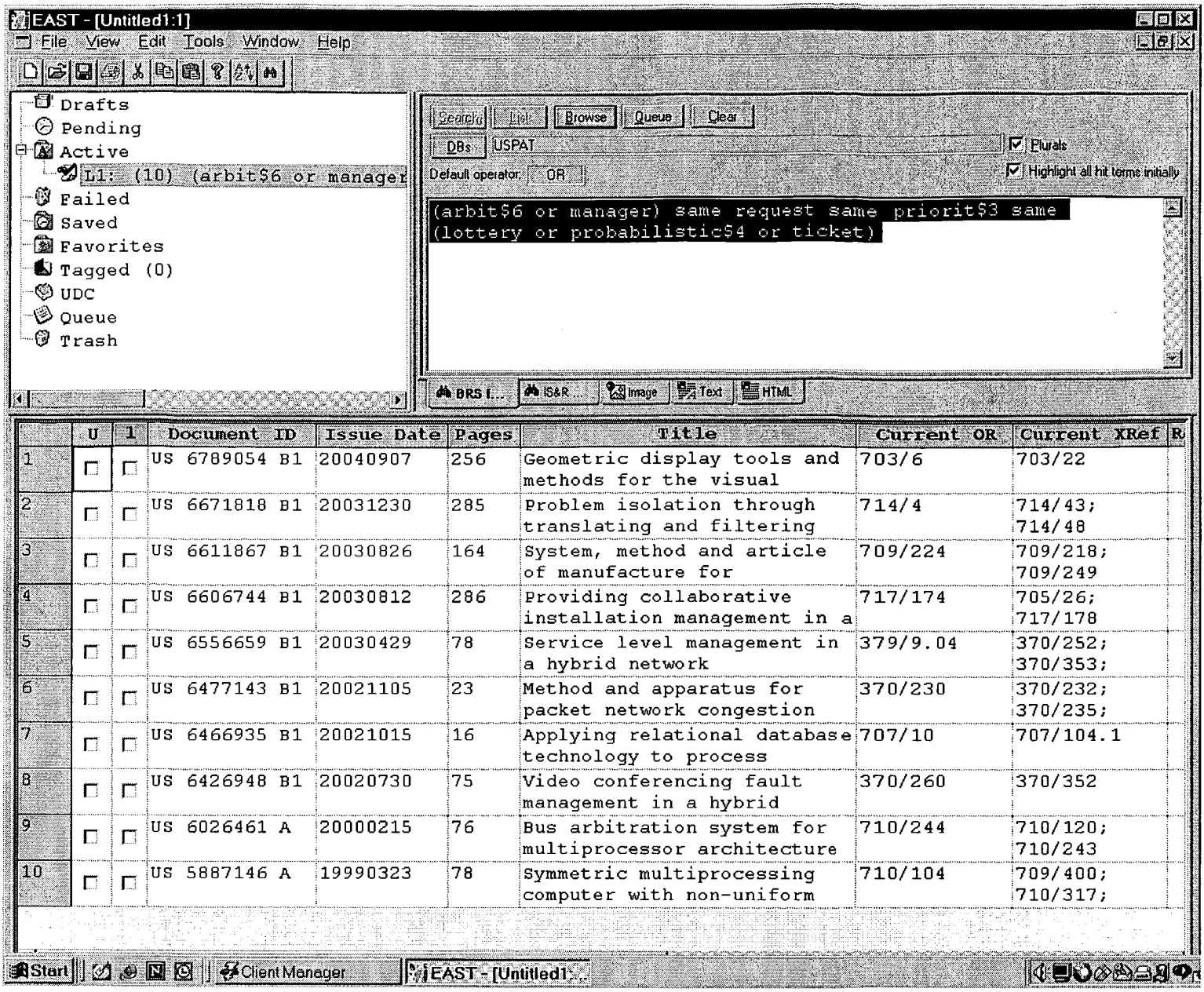


| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR | Current XRef | R |
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| 1 | ☐ | ☐ | US 6789054 B1 | 20040907 | 256 | Geometric display tools and methods for the visual | 703/6 | 703/22 | |
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| 6 | ☐ | ☐ | US 6477143 B1 | 20021105 | 23 | Method and apparatus for packet network congestion | 370/230 | 370/232; 370/235; | |
| 7 | ☐ | ☐ | US 6466935 B1 | 20021015 | 16 | Applying relational database technology to process | 707/10 | 707/104.1 | |
| 8 | ☐ | ☐ | US 6426948 B1 | 20020730 | 75 | Video conferencing fault management in a hybrid | 370/260 | 370/352 | |
| 9 | ☐ | ☐ | US 6026461 A | 20000215 | 76 | Bus arbitration system for multiprocessor architecture | 710/244 | 710/120; 710/243 | |
| 10 | ☐ | ☐ | US 5887146 A | 19990323 | 78 | Symmetric multiprocessing computer with non-uniform | 710/104 | 709/400; 710/317; | |

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1 **Performance model for a prioritized multiple-bus multiprocessor sy**
*John, L.K.; Yu-Cheng Liu;*
Computers, IEEE Transactions on , Volume: 45 , Issue: 5 , May 1996
Pages:580 - 588

[Abstract] [PDF Full-Text (724 KB)] **IEEE JNL**

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2 **Dynamic bandwidth reservation in hierarchical wireless ATM netwo using GPS-based prediction**
*Wee-Seng Soh; Kim, H.S.;*
Vehicular Technology Conference, 1999. VTC 1999 - Fall. IEEE VTS 50th , Vol 1 , 19-22 Sept. 1999
Pages:528 - 532 vol.1

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

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3 **Performance model for a prioritized multiple-bus multiprocessor sy**
*Kurian, L.; Yu-Cheng Liu;*
Parallel and Distributed Processing, 1994. Proceedings. Sixth IEEE Symposiur on , 26-29 Oct. 1994
Pages:577 - 584

[Abstract] [PDF Full-Text (488 KB)] **IEEE CNF**

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4 **Fuzzy Logic Arbiters for Multiple-Bus Multiprocessor Systems**
*Diab, H.B.;*
Systems, Man and Cybernetics, Part C, IEEE Transactions on , Volume: 34 , I 3 , Aug. 2004
Pages:281 - 292

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[Abstract] [PDF Full-Text (480 KB)] **IEEE JNL**

5 **A SoC communication architecture with fine-grained control over bandwidths and latencies**
*Xu Ningyi; Liu Hong; Zhou Zucheng; Peng Jihu;*
ASIC, 2003. Proceedings. 5th International Conference on , Volume: 1 , 21-2 2003
Pages:409 - 412 Vol.1

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# Performance model for a prioritized multiple-bus multiprocessor system

John, L.K. Yu-Cheng Liu
Dept. of Comput. Sci. & Eng., Univ. of South Florida, Tampa, FL, USA;
*This paper appears in:* **Computers, IEEE Transactions on**

Publication Date: May 1996
On page(s): 580 - 588
Volume: 45 , Issue: 5
ISSN: 0018-9340
Reference Cited: 24
CODEN: ITCOB4
Inspec Accession Number: 5294010

**Abstract:**
The performance of a shared memory multiprocessor system with a multiple-interconnection network is studied in this paper. The effect of bus and memor contention is modeled using a **probabilistic** model and a closed form solutior acceptance **probability** of each processor is presented. It is assumed that ea processor in the system has a distinct **priority** assigned to it and that **arbitra** based on **priority**. Whenever a **request** from a processor is rejected due to t memory conflicts, the **request** is resubmitted until granted. Based on the mo individual processor acceptance **probabilities** are first estimated, from which effective memory bandwidth is computed. The accuracy of the analytical mod based on simulation results. Results from the model are compared against otl approximate models previously reported in literature. It is observed that the i of the model measured in terms of error from simulation results is less than t previously reported studies

**Index Terms:**
multiprocessing systems performance evaluation shared memory systems acceptan **probabilities** acceptance **probability** **arbitration** distinct **priority** memory bandwic bus interconnection network performance **prioritized** multiple-bus multiprocessor sh multiprocessor system



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[Buy Via Ask*IEEE]

3, L.N. Bhuyan,, Q. Yang and D.P. Agrawal,, "Performance of Multiprocessor Interconnection Networks," *Computer,* vol. 22, no. 2, pp. 25-37, Feb. 1989.
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[Abstract] [PDF Full-Text (1288KB)]

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[Buy Via Ask*IEEE] [CrossRef]

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# Fuzzy Logic Arbiters for Multiple-Bus Multiprocesso Systems

Diab, H.B.

*This paper appears in:* **Systems, Man and Cybernetics, Part C, IEEE Tran on**

Publication Date: Aug. 2004
On page(s): 281 - 292
Volume: 34 , Issue: 3
ISSN: 1094-6977

**Abstract:**
This paper describes and evaluates the use of fuzzy logic **arbiters** for multipl shared memory multiprocessor system. Multiple-bus systems allow multiple a simultaneous bus transfer in addition to a high degree of fault tolerance. In s systems, **arbiters** are used to resolve conflicts to system resources, which ar shared memory modules and the buses. Typically, these conflicts are resolvec two-stage **arbitration** schemes that employ policies such as random choice, chaining, round-robin, etc. A new way of implementing these **arbiters** is the logic to resolve resource **request** conflicts based on the system state and per variables. This paper describes a new technique for implementation of fuzzy l system **arbiters** and presents a simulation program that evaluates the syster performance. The program is coded in such a way as to accommodate any **ar** scheme, from which the fixed **priority** and fuzzy **priority** have been impleme Parameters affecting multiple-bus system performance are considered and us to the fuzzy **arbiters**. The inputs are fuzzified by using appropriate membersl functions, and rules have been defined in such a way as to increase and distri the acceptance **probability** of each processor in the system. Results from the program using a **prioritized arbitration** scheme are compared against other results and show very close agreement. Furthermore, results show an increas acceptance **probability** of the processors using fuzzy **arbiters**.

**Index Terms:**
Fuzzy control fuzzy logic multiple-bus **arbiters** multiprocessor systems performanc

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L1: Entry 1 of 6 File: PGPB Jun 24, 2004

PGPUB-DOCUMENT-NUMBER: 20040122735
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040122735 A1

TITLE: System, method and apparatus for an integrated marketing vehicle platform

PUBLICATION-DATE: June 24, 2004

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY | RULE-47 |
|---|---|---|---|---|
| Meshkin, Alexander B. | Columbia | MD | US | |

US-CL-CURRENT: 705/14; 705/10

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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L1: Entry 2 of 6 File: PGPB Dec 4, 2003

PGPUB-DOCUMENT-NUMBER: 20030222603
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030222603 A1

TITLE: Multiple channel ballast and networkable topology and system including power line carrier applications

PUBLICATION-DATE: December 4, 2003

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY | RULE-47 |
|---|---|---|---|---|
| Mogilner, Rafael | Rehovot | | IL | |
| Nogtev, Boris | Rishon Lezion | | IL | |
| Kuchlik, Yuri | Sderot | | IL | |
| Rubin, Daniel | Ness Ziona | | IL | |
| Lev, Arie | Mazkeret Batya | | IL | |
| Rabinovitz, Eytan | Rishon Lezion | | IL | |

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US-CL-CURRENT: 315/294; 315/292, 315/312

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 3. Document ID: US 20030188065 A1

L1: Entry 3 of 6 File: PGPB Oct 2, 2003

PGPUB-DOCUMENT-NUMBER: 20030188065
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030188065 A1

TITLE: Binary tree arbitration system and method

PUBLICATION-DATE: October 2, 2003

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY | RULE-47 |
|---|---|---|---|---|
| Golla, Prasad N. | Plano | TX | US | |
| Damm, Gerard | Dallas | TX | US | |
| Ozugur, Timucin | Garland | TX | US | |
| Blanton, John | Dallas | TX | US | |
| Verchere, Dominique | Plano | TX | US | |

US-CL-CURRENT: 710/243

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 20020129181 A1

L1: Entry 4 of 6 File: PGPB Sep 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020129181
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020129181 A1

TITLE: High-performance communication architecture for circuit designs

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY | RULE-47 |
|---|---|---|---|---|
| Lahiri, Kanishka | Princeton | NJ | US | |
| Raghunathan, Anand | Princeton | NJ | US | |
| Lakshminrayana, Ganesh | Princeton | NJ | US | |

US-CL-CURRENT: 710/113

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6789054 B1

L1: Entry 5 of 6 File: USPT Sep 7, 2004

US-PAT-NO: 6789054
DOCUMENT-IDENTIFIER: US 6789054 B1

TITLE: Geometric display tools and methods for the visual specification, design automation, and control of adaptive real systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Drawi De

☐ 6. Document ID: US 6477143 B1

L1: Entry 6 of 6 File: USPT Nov 5, 2002

US-PAT-NO: 6477143
DOCUMENT-IDENTIFIER: US 6477143 B1

TITLE: Method and apparatus for packet network congestion avoidance and control

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Drawi De

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| (arbit$6 or manager) same request same priorit$3 same (lottery or probabilistic$4) | 6 |

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PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020129181 A1

TITLE: High-performance communication architecture for circuit designs

PUBLICATION-DATE: September 12, 2002

INVENTOR-INFORMATION:

| NAME | CITY | STATE | COUNTRY | RULE-47 |
|---|---|---|---|---|
| Lahiri, Kanishka | Princeton | NJ | US | |
| Raghunathan, Anand | Princeton | NJ | US | |
| Lakshminrayana, Ganesh | Princeton | NJ | US | |

ASSIGNEE-INFORMATION:

| NAME | CITY | STATE | COUNTRY | TYPE CODE |
|---|---|---|---|---|
| NEC USA, INC. | | | | 02 |

APPL-NO: 09/ 874323 [PALM]
DATE FILED: June 6, 2001

RELATED-US-APPL-DATA:
Application is a non-provisional-of-provisional application 60/259218, filed January 3, 2001,

INT-CL: [07] G06 F 13/36

US-CL-PUBLISHED: 710/113
US-CL-CURRENT: 710/113

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A circuit comprising a plurality of components sharing at least one shared resource, and a lottery manager. The lottery manager is adapted to receive request for ownership for said at least one shared resource from a subset of the plurality of components. Each of the subset of the plurality of components are assigned lottery tickets. The lottery manager is adapted to probabilistically choose one component from the subset of the plurality of components for assigning said at least one shared resource. The probabilistic choosing is weighted based on a number of lottery tickets being assigned to each of the subset of the plurality of components.

I. RELATED APPLICATIONS

[0001] This Application claims priority from co-pending U.S. Provisional Application Serial No. 60/259,218, filed Jan. 3, 2001.

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L5: Entry 3 of 3 File: USPT Feb 15, 2000

DOCUMENT-IDENTIFIER: US 6026461 A
TITLE: Bus arbitration system for multiprocessor architecture

Brief Summary Text (26):
The motherboard level PIX busses each use a centralized arbitration scheme wherein each bus requester sends the ORB ASIC information about the requested packet type and about the state of its input queues. The ORB ASIC implements a fairness algorithm and grants bus requests based on such information received from requesters, and based on other information sampled from requesters. The ORB samples a mix of windowed and unwindowed requesters every bus clock cycle. Windowed requests have associated therewith particular time periods during which the request signal must be sampled and a grant issued and prioritized in accordance with predetermined parameters. At the same time that PIX bus requesters are being sampled, the ORB samples the busy signals of the potential bus targets. During the cycle after sampling, the ORB chooses one low priority requester, one medium priority requester and one high priority requester as potential bus grant candidates, based on: ordering information from a low and a medium request tracking FIFO; the state of the Busy signals sampled; and a "shuffle code" which ensures fairness of bus grants. Further selection for a single candidate for the PIXbus grant involves a prioritization algorithm in which high priority requests have priority over medium requests which have priority over low, and in which medium level requests are subjected to a "deli-counter-ticket" style prioritization scheme that maintains time ordering of transactions. High and low priority requests are not strictly granted based on time ordering.

Current US Original Classification (1):
710/244

Current US Cross Reference Classification (2):
710/243

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L5: Entry 3 of 3 File: USPT Feb 15, 2000

US-PAT-NO: 6026461
DOCUMENT-IDENTIFIER: US 6026461 A

TITLE: Bus arbitration system for multiprocessor architecture

DATE-ISSUED: February 15, 2000

INVENTOR-INFORMATION:

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APPL-NO: 09/ 208139 [PALM]
DATE FILED: December 9, 1998

PARENT-CASE:
RELATED APPLICATION This application is a divisional application of U.S. application Ser. No. 08/695,556, filed on Aug. 12, 1996, now U.S. Pat. No. 5,887,146. The present application claims the benefit of U.S. Provisional Application No. 60/002,320, filed Aug. 14, 1995, which is hereby incorporated

herein by reference.

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 710/244; 710/243, 710/120
US-CL-CURRENT: 710/244; 710/120, 710/243

FIELD-OF-SEARCH: 710/107, 710/111-118, 710/240, 710/241, 710/243, 710/244

PRIOR-ART-DISCLOSED:

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Search Selected | Search ALL | Clear

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ART-UNIT: 271

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ABSTRACT:

A very fast, memory efficient, highly expandable, highly efficient CCNUMA processing system based on a hardware architecture that minimizes system bus contention, maximizes processing forward progress by maintaining strong ordering and avoiding retries, and implements a full-map directory structure cache coherency protocol. A Cache Coherent Non-Uniform Memory Access (CCNUMA) architecture is implemented in a system comprising a plurality of integrated modules each consisting of a motherboard and two daughterboards. The daughterboards, which plug into the motherboard, each contain two Job Processors (JPs), cache memory, and input/output (I/O) capabilities. Located directly on the motherboard are additional integrated I/O capabilities in the form of two Small Computer System Interfaces (SCSI) and one Local Area Network (LAN) interface. The motherboard includes main memory, a memory controller (MC) and directory DRAMs for cache coherency. The motherboard also includes GTL backpanel interface logic, system clock generation and distribution logic, and local resources including a micro-controller for system initialization. A crossbar switch connects the various logic blocks together. A fully loaded motherboard contains 2 JP daughterboards, two PCI expansion boards, and up to 512 MB of main memory. Each daughterboard contains two 50 MHz Motorola 88110 JP complexes, having an associated 88410 cache controller and 1 MB Level 2 Cache. A single 16 MB third level write-through cache is also provided and is controlled by a third level cache controller.

8 Claims, 41 Drawing figures

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US-CL-CURRENT: 710/244; 710/120, 710/243

FIELD-OF-SEARCH: 710/107, 710/111-118, 710/240, 710/241, 710/243, 710/244

Previous Doc Next Doc Go to Doc#

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US006026461A

# United States Patent [19]

Baxter et al.

[11] Patent Number: 6,026,461

[45] Date of Patent: Feb. 15, 2000

[54] **BUS ARBITRATION SYSTEM FOR MULTIPROCESSOR ARCHITECTURE**

[75] Inventors: William E. Baxter, Hollliston; Robert G. Gelinas, Westboro; James M. Guyer, Northboro; Dan R. Hinds, Shrewsbury; Michael F. Hunt, Ashland; David L. Keating, Holliston, all of Mass.; Jeff S. Kimmell, Chapel Hill, N.C.; Phil J. Roux, Holliston, Mass.; Liz M. Trusebusch, Sudbury, Mass.; Rob P. Valentine, Auburn, Mass.; Pat J. Weller, Northboro, Mass.; Joseph Cox, Middleboro, Mass.; Barry E. Gillott, Fairport, N.Y.; Andrea Heyda, Acton, Mass.; Rob J. Pike, Northboro, Mass.; Tom V. Hadingue, Westboro, Mass.; Art A. Sherman, Maynard, Mass.; Michael Sporer, Wellesley, Mass.; Doug J. Tucker, Northboro, Mass.; Simon N. Yeung, Waltham, Mass.

[73] Assignee: Data General Corporation, Westboro, Mass.

[21] Appl. No.: 09/208,139

[22] Filed: Dec. 9, 1998

**Related U.S. Application Data**

[62] Division of application No. 08/595,556, Aug. 12, 1996, Pat. No. 5,887,146.

[60] Provisional application No. 60/002,320, Aug. 14, 1995.

[51] Int. Cl.[7] ..... G06F 13/14

[52] U.S. Cl. ..... 710/244; 710/243; 710/120

[58] Field of Search ..... 710/107, 111–118, 710/240, 241, 243, 244

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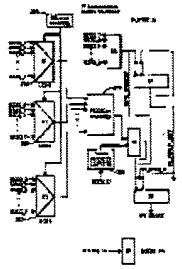
[57] **ABSTRACT**

A very fast, memory efficient, highly expandable, highly efficient CCNUMA processing system based on a hardware architecture that minimizes system bus contention, maximizes processing forward progress by maintaining strong ordering and avoiding retries, and implements a full-map directory structure cache coherency protocol. A Cache Coherent Non-Uniform Memory Access (CCNUMA) architecture is implemented in a system comprising a plurality of integrated modules each consisting of a motherboard and two daughterboards. The daughterboards, which plug into the motherboard, each contain two Job Processors (JPs), cache memory, and input/output (I/O) capabilities. Located directly on the motherboard are additional integrated I/O capabilities in the form of two Small Computer System Interfaces (SCSI) and one Local Area Network (LAN) interface. The motherboard includes main memory, a memory controller (MC) and directory DRAMs for cache coherency. The motherboard also includes GTL backpanel interface logic, system clock generation and distribution logic, and local resources including a micro-controller for system initialization. A crossbar switch connects the various logic blocks together. A fully loaded motherboard contains 2 JP daughterboards, two PCI expansion boards, and up to 512 MB of main memory. Each daughterboard contains two 50 MHz Motorola 88110 JP complexes, having an associated 88410 cache controller and 1 MB Level 2 Cache. A single 16 MB third level write-through cache is also provided and is controlled by a third level cache controller.

**8 Claims, 38 Drawing Sheets**



US006556659B1

(12) **United States Patent**
**Bowman-Amuah**

(10) **Patent No.: US 6,556,659 B1**
(45) **Date of Patent: Apr. 29, 2003**

(54) **SERVICE LEVEL MANAGEMENT IN A HYBRID NETWORK ARCHITECTURE**

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( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/323,015**

(22) Filed: **Jun. 2, 1999**

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(58) Field of Search ..... 379/1, 9, 10, 14, 379/15, 32, 33, 34, 113, 115, 133, 134, 207, 219; 370/232, 244, 252, 253, 352, 353; 709/224, 250; 707/10

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(57) **ABSTRACT**

A Service Level Management system is provided. A notification of a service level problem within a combination packet-switching and circuit-switching hybrid network is received by the system. The service level agreement is retrieved and the problem is checked against the agreement to determine if the agreement has been met. The notification of the problem is prioritized with a second notification of a second service level problem based on a number of times the agreement has not been met. Next, a resolution for the service level problem within the hybrid network is determined. The resolution may include a status report, resolution notification, problem reports, service reconfiguration, trouble notification, service level agreement violations, and/or outage notification. The progress of the implementation of the resolution is tracked. Finally, the hybrid network is managed based on the future predicted behavior of the network.

**13 Claims, 43 Drawing Sheets**